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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,924	10/10/2001	Albrecht Mayer	J&R-0748	1097

24131 7590 08/11/2005

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EXAMINER	
RIZZUTO, KEVIN P	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,924	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/24/05 and 7/14/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Request for Continued Examination as received on 6/24/2005 and 7/14/2005.

New Claim Objections

3. Claim 10 is objected to for the following minor informalities: duplicate period at the end of the claim. Appropriate correction is required.

Withdrawn Rejections

4. Applicant has overcome the 35 U.S.C. 102 and 103 rejections set forth in the previous Office Action for claims 1-17 via amendments. Therefore, these rejections are withdrawn by the examiner.

New Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 10-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2.

7. Regarding claim 1, Harrison, has taught a programmable unit, comprising:

a. At least one program operation unit for running a program [Processor 16 (PO 16), fig. 1 and col. 3, lines 11-19]

b. A stopping device (bus monitor 12, figures 1 and 2) connected to said program operation unit said stopping device stopping the running of the program by said program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

c. Other components [P1-P7, fig. 1] connected to said stopping device said stopping device also issuing a stop command causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

d. And said other components including at least one further program operation unit or at least one peripheral [P1-P7, fig. 1], said stopping command being selectively provided from said stopping device to said other component if said other component is said further program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

e. And said stop command being directly provided from said stopping device to said other component if said other component is a peripheral:

[Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

f. Examiner notes that the claim language only requires the other components to be *either* a further program operation unit *or* a peripheral, *not both.* However, The American Heritage Dictionary of the English Language, 4th Ed defines peripheral as, "An auxiliary device, such as a printer, modem, or storage system, that works in conjunction with a computer." It then defines auxiliary as, 1. Giving assistance or support; helping." A processor within a multiprocessor system is a peripheral to the other processors, and the other processors are peripherals to the processor, since each works in conjunction with a computer giving assistance or support to carry out data processing. Therefore, any of the processors, P1-P7 could be considered either a peripheral or a program operation unit.

8. However, Harrison has not taught wherein said stopping device is located on the same chip as said program operation unit.

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the bus monitor 12 and the PO 16 onto a single chip since it has been held "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice." [In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)]

10. Given the similarities between the claims, the arguments as stated for claim 1 are also applicable to claim 11.

11. Regarding claim 2, Harrison has taught the programmable unit according to claim 1, wherein said other components [P1-P7, fig.1] include at least one further program operation unit and said stopping device able to stop said further program operation unit which is not associated with said stopping device. [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

12. Regarding claim 3, Harrison has taught the programmable unit of claim 2, wherein said other components [P1-P7, fig. 1] which can be stopped by said stopping device include units which are connected to and cooperate with said program operation unit and said further program operation unit: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

13. Regarding claim 4, Harrison has taught the programmable unit of claim 3, wherein said units are stopped by said stopping device later in time than said program operation unit and said further program operation unit: [The processors (P1-P7) can be selectively stopped, depending on the settings within bus monitor 12. The settings are alterable, i.e., the bus monitor can be set up to issue stop commands to certain processors at one point during processing, then the set-up can be altered so that different processors are issued the stop command. [Fig. 5, and col. 9, lines 17-35] Therefore, some units (e.g., PO 3 and 4) can be initially not given the stop command upon a first breakpoint. Then, the bus monitor 12 can be reconfigured so that upon another breakpoint (later in time), the units (PO 3 and 4) will be issued a stop command.]

14. Given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 12.

15. Regarding claim 5, Harrison has taught the programmable unit of claim 4, including at least one bus connected between said other components [Figure 1]

16. Given the similarities between the claims, the arguments as stated for claim 5 are also applicable to claim 13.

17. Regarding claim 6, Harrison has taught the programmable unit of claim 5, including bus interfaces and each of said bus interfaces is connected to one of said program operation unit and said further program running unit and to said bus: The program operation unit [P0] and further program running unit [Any of [P1-P7]: Each of the processors [P0-P7] is connected to a bus as shown in figure 1, [Shared-Memory Bus 15]. Interface is defined as, "A surface forming a common boundary between adjacent regions, bodies, substances, or phases. 2. A point at which independent systems or diverse groups interact. 3. *Computer Science* a. The point of interaction or communication between a computer and any other entity, such as a printer or human operator." (The American Heritage College Dictionary, 4th Edition) Therefore, since the bus is connected to both the program operation unit and said further program running unit, there is an interface present at the connection point, in which both the bus and the program operation unit or said further program unit are connected.

-Said program operation unit and said further program operation unit function as bus masters: [Each of the processors (P0-P7) operate as bus masters since each has memory controller. When a processor has access to the

shared bus to communicate with the shared memory (Read or Write), it is functioning as a bus master. Col. 3, lines 20-34, figure 1.]

18. Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach where said units are stopped only when said bus masters and said bus interfaces have no more data to output and/or are no longer waiting for already requested data or data that is still to be requested.

19. One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level associated with the stop command (breakpoint interrupts) so as to allow the bus masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

20. Given the similarities between the claims, the arguments as stated for claim 6 are also applicable to claim 14.

21. Regarding claim 7, Harrison has taught the programmable unit according to claim 5, wherein said bus includes a first bus part, a second bus part and a bus bridge connecting said first bus part to said second bus part: [Figure 1. Each vertical line portion of Shared – Memory Bus 15 is a "bus part". The horizontal line portion of Shared – Memory Bus 15 is the "bus bridge" connecting said first bus part to said second bus part.]

22. Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach wherein said units are stopped only when said bus bridge has no more data to pass on.

23. One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level associated with the stop command

(breakpoint interrupts) so as to allow the bus masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

24. Given the similarities between the claims, the arguments as stated for claim 7 are also applicable to claim 15.

25. Regarding claim 10, Harrison has taught the programmable unit of claim 1, wherein said stopping device is an on-chip debug support module. [It is inherent that the stopping device (bus monitor 12) is designed/made on a chip because it contains hardware and logic as shown in figure 2. Harrison discloses there the bus monitor device is used for debugging and monitoring. [Col. 3, line 42 to col. 4, line 39]

26. Given the similarities between the claims, the arguments as stated for claim 10 are also applicable to claim 17.

27. Claims 8, 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2, and further in view of Wen et al., U.S. Patent 5,956,514, herein referred to as Wen.

28. Regarding claim 8, Harrison has taught the programmable unit of claim 1, but does not give a thorough disclosure of the restarting of the application on the parallel processors (P0-P7). Harrison only states that the Processor 16 (P0) runs the debugging program and it issues a command to resume execution of the application when the debugging is completed. Therefore, processor 16 (P0) is the master processor, and the others are slaves.

29. However, Harrison fails to teach wherein after a stopped state of components of the programmable unit which have been stopped is cancelled,

said units recommence operation before said program operation unit and said further program operation unit recommence operation.

30. Wen teaches wherein after a breakpoint, and debugging, the Master processor can issue a restart command [unhold_cpu()] to individual slave processors. The restart command can either indicate to start the application over from the beginning or to resume at the point from which it was interrupted at. This allows a greater degree of flexibility for the programmer, because it is possible to selectively restart processors. [Col. 6, lines 41-64 and figure 1] This is similar to Harrison's teaching for selectively issuing the stop commands, which has the of increased flexibility for debugging purposes. Adding this feature to Harrison would cause the P0 processor to cause the "units" to recommence processing before the P0 processors does, and also at different times from each other. Therefore, the restarting command would cause the "units" to recommence operation before said program operation unit and said further program operation unit.

31. It would have been obvious to one of ordinary skill in the art to use the teachings of Wen, wherein slave processors can be selectively resumed, since it would increase the flexibility of the debugging process.

32. Regarding claims 9 and 16, given the similarities between claim 8 and claims 9 and 16, the arguments as stated for claim 8 are also applicable to claims 9 and 16.

Response to Remarks

33. Applicant's arguments filed on 23 December 2004, have been fully considered but they are moot in view of the new rejections above, which were necessitated by the amendments to the claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of art disclosed by the references cited and the objections made. Applicant must show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

15. Inquiries concerning this communication or earlier communications from the examiner should be directed to Kevin Rizzuto who can be reached at (571) 272-4174. The examiner can normally be reached between the hours 9:00am – 5:30pm (EST), Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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